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G02F 1/025

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G2F FCW F23E

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GB 2340616 A GB 2265252 A

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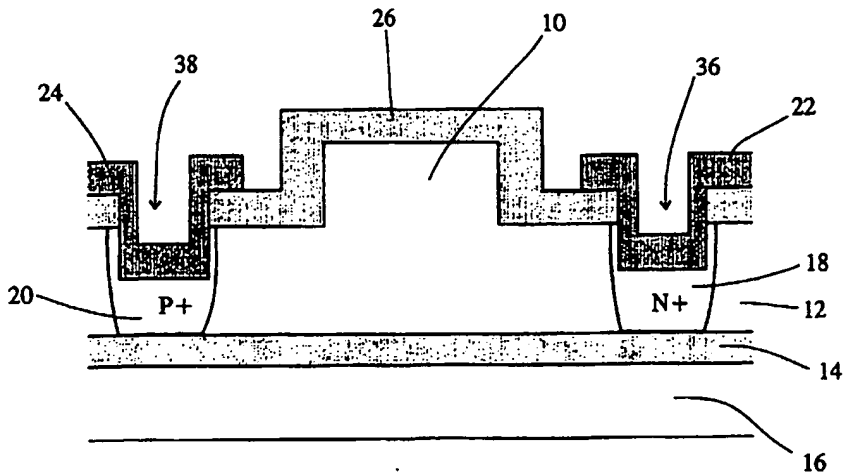
(54) Abstract Title
Electro-Optic Modulator

(57) An electro-optic device includes a semiconducting layer 12 in which is formed a waveguide 10 a modulator formed across the waveguide comprising a p-doped region 20 to one side and an n-doped region 18 to the other side of the waveguide, wherein at least one of the doped regions extends from the base of a recess 36, 38 formed in the semiconducting layer. In this way, the doped regions can extend further into the semiconducting layer and further hinder escape of charge carriers without the need to increase the diffusion distance of the dopant and incur an additional thermal burden on the device. In an SOI device, the doped region can extend to the insulating layer 14. Ideally, both the p and n-doped regions extend from the base of a recess, but this may be unnecessary in some designs. Insulating layers can be used to ensure that dopant extends from the base of the recess only, giving a more clearly defined doped region. The (or each) recess can have non-vertical sides, such as are formed by v-groove etches, A combination of a vertical sidewall at the base of the recess and a non-vertical sidewall at the opening could be used.

Fig 4



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

GB 2 372 576 A

Fig 1

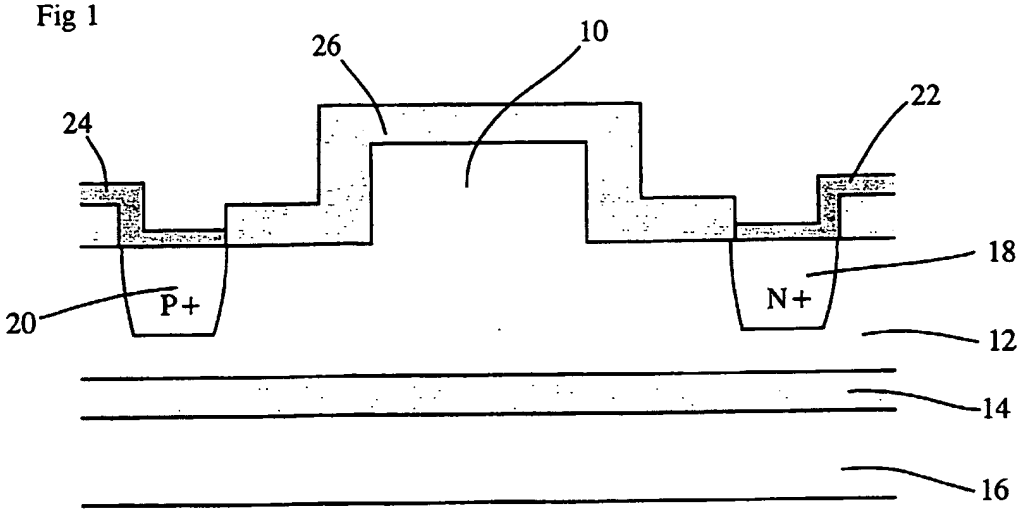


Fig 2a

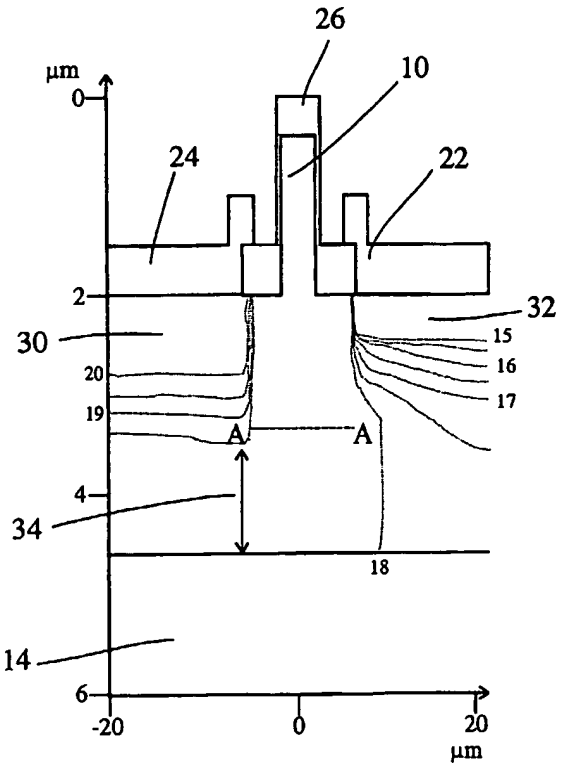


Fig 2b

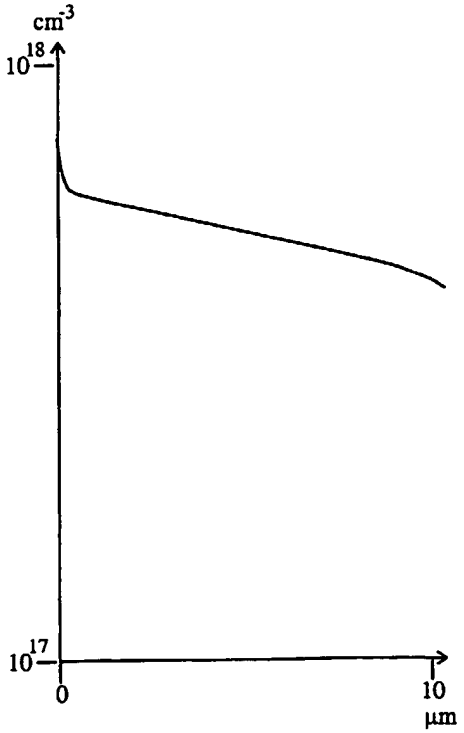


Fig 3

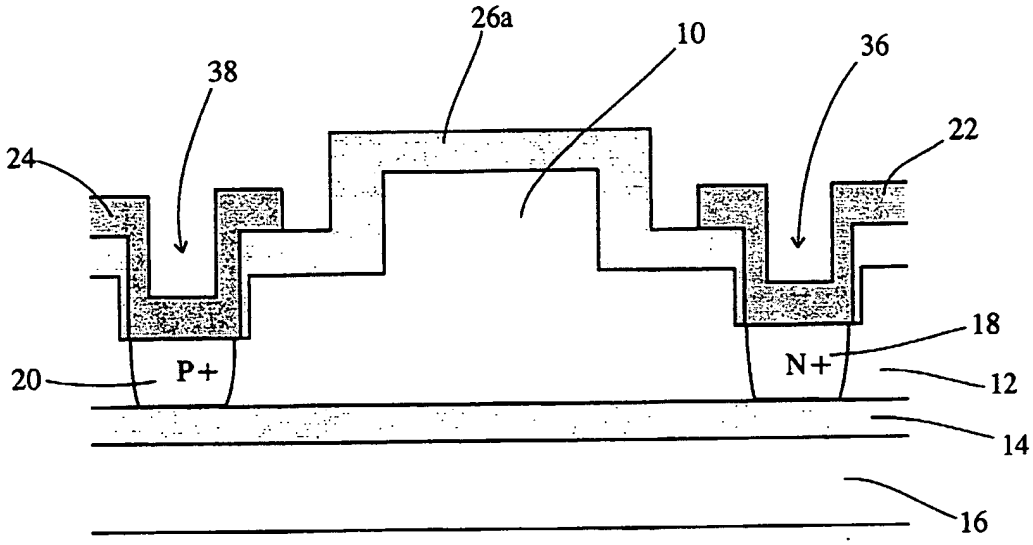


Fig 4

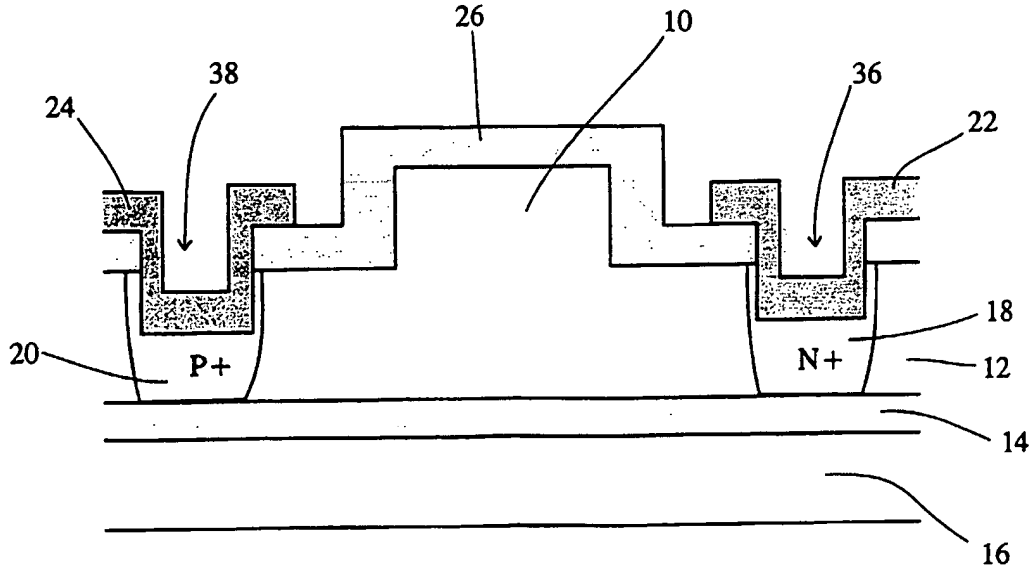


Fig 5a

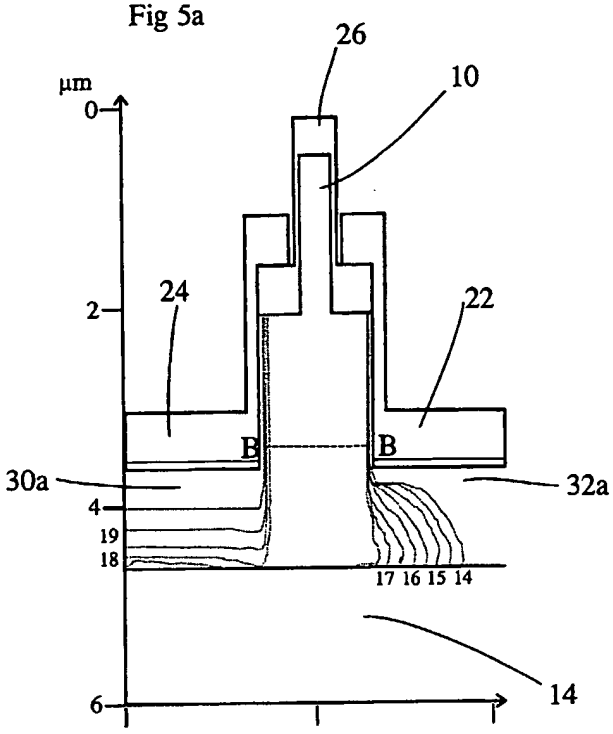


Fig 5b

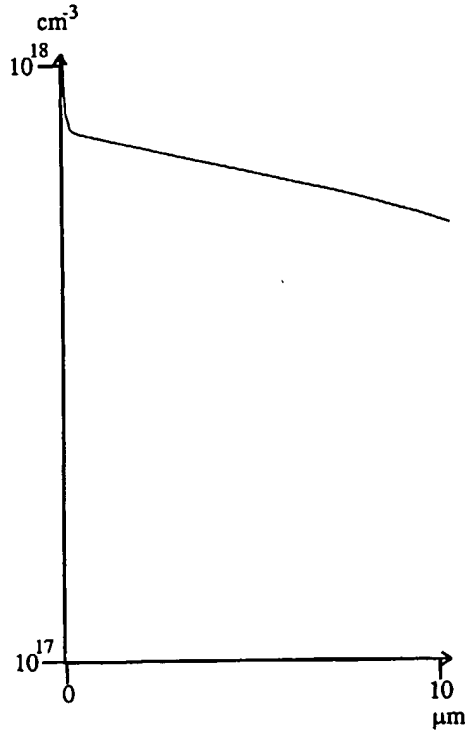


Fig 5c

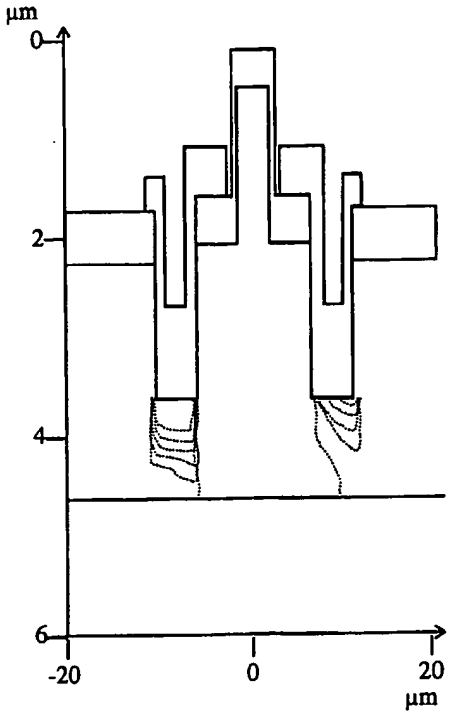


Fig 6

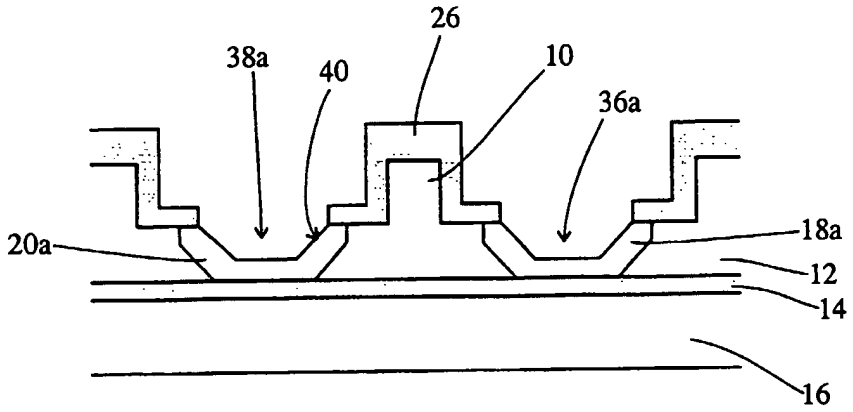
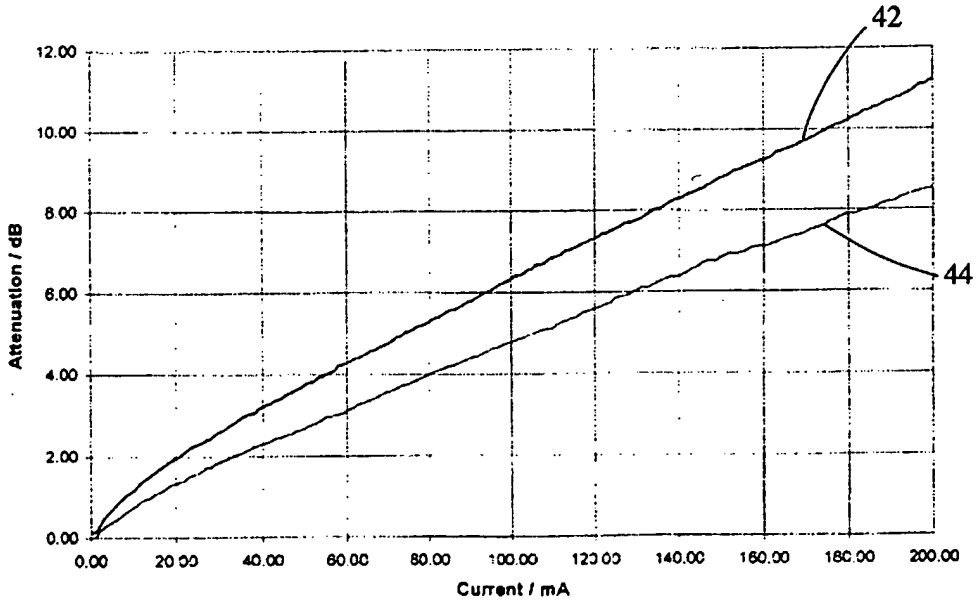

26
38a
40
10
36a
20a
18a
12
14
16

Fig 7


42
44
12.00
10.00
8.00
6.00
4.00
2.00
0.00
Attenuation / dB
0.00
20.00
40.00
60.00
80.00
100.00
120.00
140.00
160.00
180.00
200.00
Current / mA

ELECTRO-OPTIC MODULATOR

The present invention relates to an electro-optic modulator.

Electro-optic modulators influence an optical mode and are understood to work by affecting the complex refractive index of a semiconductor waveguide and thereby affecting the transmission of light propagating therein. In such a device, a p-i-n diode formed across the waveguide and injects charge carriers into the region in which the mode is propagating. The presence of significant numbers of charge carriers affects the local refractive index and thus the speed of light transmission. This effect can be used in switches, interferometers etc.

In SOI optical devices the mod propagates in a silicon layer over an insulating layer supported on a substrate. The insulating layer can then act as a confinement layer for the charge carriers in the vertical direction. However, it has been found that significant numbers of charge carriers still escape laterally, and this adversely affects both the performance of the device and its reproducibility.

The present invention therefore provides, in its first aspect, an electro-optic device including a semiconductor layer in which is formed a waveguide, a modulator formed across the waveguide comprising a doped region on either side,

a lower confinement structure for charge carriers beneath the waveguide, lateral confinement structures for charge carriers on either side of the waveguide which extend to the lower confinement structure, at least one of the lateral confinement structures being the doped region to that side of the waveguide, the doped region extending to the lower confinement structure.

It is preferred that the semiconducting layer is formed on an insulating layer supported on a substrate, i.e. an SOI device. In this case, the insulating layer can provide the lower confinement structure.

It is naturally preferred that both lateral confinement structures are provided by the respective p and n-doped regions either side of the waveguide. However, there may at times be no need or no motivation to do so on one particular side, for example if there are adjacent structures which themselves may provide electrical confinement.

The lateral confinement structures and/or the doped regions (where the two are distinct) can extend from the base of a recess in the semiconducting layer to the insulating layer.

The waveguide is normally covered by an insulating layer to ensure a distinct refractive index step, confining the optical mode, and to reduce unwanted electrical effects. This insulating layer can extend to and down at least one side of the recess, which if put in place prior to doping will ensure that dopant extends from the base of the recess only, giving a more clearly defined doped region.

The (or each) recess can have non-vertical sides, such as are formed by v-groove etches, which method of manufacture has the advantage that metal contacts leading to the doped regions will be less prone to failure due to thinning at the edge of the recess. A combination of a vertical sidewall at the base of the recess and a non-vertical sidewall at the opening could be used.

In a standard lateral p-i-n diode structure, the doped region to one side is p-type and the doped region to the other side of the waveguide is n-type. Other diode geometries exist, however, and other electrical structures such as transistors can be provided.

Confining structures are used in the present invention to inhibit the escape of charge carriers from the region of interest. Physical structures such as deep trenches, insulating layers and the like will provide confinement. In addition, we have found that a doped region provides confinement. It is thought that opposite charges are confined by a recombination process and like charges are confined by the concentration gradient established by the dopant.

In its second aspect, the present invention provides an electro-optic device including a semiconducting layer in which is formed a waveguide, a modulator formed across the waveguide comprising a doped region on either side, wherein at least one of the doped regions extends from the base only of a recess formed in the semiconducting layer.

In this way, the doped regions can extend further into the semiconducting layer and further hinder escape of charge carriers laterally within the semiconductor layer. This is however achieved without the need to increase the diffusion distance of the dopant, which would incur an additional thermal burden on the device. Further, limitation of the dopant area to the base of the recess reduces the lateral spread of dopant and keeps the volume used for transmission of the optical mode clear of dopant, which if present is apt to cause losses and inefficiency.

As before, an oxide layer can be provided on side walls of the device to inhibit diffusion of dopant therethrough. Alternatively, or in addition, the dopant can be implanted in the semiconducting layer.

The waveguide is preferably a rib waveguide, although other designs of waveguide are known and can be used.

A plurality of such lateral modulators can be formed along the length of the waveguide, each being a p-i-n modulator, adjacent modulators being mutually reversed in orientation. This gives a particularly efficient form of modulation. Ideally there will be an even number of modulators such as four.

Embodiments of the present invention will now be described by way of example, with reference to the accompanying figures, in which;

Figure 1 is a vertical section through a known lateral p-i-n diode modulator;

Figure 2a is a model of the carrier density of the modulator of figure 1;

Figure 2b is a plot of the carrier concentration along line A-A of figure 2a;

Figures 3 and 4 are vertical sections through p-i-n diode modulators being first and second embodiments of the present invention;

Figure 5a is a model of the carrier density of the modulator of figure 4;

Figure 5b is a plot of the carrier concentration along line B-B of figure 5a;

Figure 5c is a model of the carrier density of the modulator of figure 3;

Figure 6 is a vertical section through a p-i-n diode modulator according to a third embodiment of the present invention; and

Figure 7 compares the attenuation of the modulator of figure 1 with the modulator of figure 6.

Figure 1 shows a standard SOI (silicon-on-insulator) rib waveguide with a lateral injection p-i-n diode made by diffusion into a semiconducting slab. In this arrangement, the waveguide 10 is in the form of a rib on the surface of the silicon epi layer 12. The epi layer 12 is formed on an insulating oxide layer 14 which is

itself supported on a substrate 16. On either side of the rib waveguide 10 are a pair of doped regions. To one side there is an n^+ doped area 18, and to the other there is a p^+ doped area 20. Metal contacts, 22, 24 lead to the doped regions 18, 20 and a p-i-n diode is thus formed. An insulating layer 26, eg of silicon dioxide, is formed over the rib waveguide 10 to provide a more distinct refractive index step and thereby assist in optical confinement, and also beneath the metal contacts 22, 24 away from the doped regions 18, 20 to provide electrical insulation.

Figure 2 shows a model of the carrier distribution for this device. In the upper region of the graph, the physical structure of the device can be seen in terms of the rib 10, the insulating layer 26 and the metal contacts 22, 24. Within the semi-conducting area, the concentration of holes is shown by way of contour lines; the peak hole concentration is 10^{20} at point 30 and the minimum is 10^{14} at 32. Contours in the intermediate regions are on a logarithmic scale. Details of the electron concentration are not shown as the device is symmetrical and therefore the hole and electron concentrations will be complementary.

It can be seen that in the doped regions 30, 32 there is a significant working concentration of charge carriers. However, there is a distinct gap 34 beneath the doped regions but above the insulating layer 14 where the charge carrier concentration is at a high level, and almost equal to the carrier concentration in the core of the waveguide. This modulation structure is therefore inefficient due to the lack of carrier confinement and poor overlap between the generated high carrier concentration and the optical mode.

Figure 2b shows the charge concentration in the area of the optical mode, and on the logarithmic scale it can be seen that the general charge carrier concentration is at approximately $5\text{-}6\times10^{17}$ cm^{-3}.

Figure 3 shows the first embodiment of the invention. The rib waveguide 10 is again formed on the silicon epi layer 12 of the SOI structure. However, a pair

of trenches 36, 38 are formed either side of the rib waveguide 10 and doping is carried out into these trenches to form an n^+ doped area 18 and a p^+ doped area 20. Metal contacts 22, 24 are again provided, as is a protective and insulating oxide layer 26.

The increased depth from which the doping is carried out, due to the trenches 36, 38, means that the n^+ and p^+ doped areas 18, 20 reach the insulating layer 14 beneath the silicon epi layer 12.

Figure 4 shows a similar structure according to a second embodiment of the invention. In the first embodiment of figure 3, doping is carried out so as to extend from the base of the recesses 36, 38 only. In figure 4, this limitation of the extent of doping is not present. These examples could be achieved (for example) by diffusion processes or by ion implantation. In figure 3, the protective oxide layer 26a is extended to the sides of the recesses 36, 38 in order to assist in limiting the doped area to the base of the trench.

The dopant profile of figure 3 is very advantageous. As the dopant extends only from the base of the trench and not from the sides, the lateral spread of the dopant during drive-in is significantly limited. In addition, the use of the recess from which the dopant extends reduces the amount of drive-in needed, and thus further reduces the lateral spread. Thus, the lateral dimension is more reproducible and more accurately ascertainable. Dopant concentrations in the vicinity of the optical mode can be avoided, reducing losses and inefficiency. The doped regions can be safely moved closer to the optical mode, thereby reducing the dimensions of the device with the attendant advantages thereof.

Figure 5a shows a model of the structure of figure 4, displayed on the same basis as figure 2a. It can be seen that the areas 30a, 32a of greatest carrier concentration are confined in the structure in that they extend to the underlying insulator layer 14. Thus, carrier escape is prevented in this arrangement and carrier

loss must therefore be by recombination. Figure 5b shows carrier concentration in the area of the optical mode, and it can be seen that on the logarithmic scale this varies between 7 and $8x10^{18}\,cm^{-3}$, a detectably higher level than that of figure 2b indicating the carriers are not escaping to the same extent.

Figure 5c shows a similar model for the structure of figure 3. It can be seen that there is little lateral escape of charge carriers, and little spread of dopant into the optical mode region.

Figure 6 shows a third embodiment of the present invention. This corresponds generally to that of figure 4 but the trench recesses 36a, 38a are formed with angled edges such as that at 40. This can be achieved via a v-groove etch, for example. This eases the deposition of the metal contacts (not shown in figure 6) as they do not need to traverse a sharp corner and are therefore less prone to thinning. Dopant can be confined to the base of the trench if desired.

In order to compare the performance advantage by employing the present invention, a device was fabricated according to figure 6 with a 1.8 micron etch on a 2.6 micron slab. A second device was fabricated identically except that the diodes were placed on the surface of the slab region as per figure 1. Doping was introduced into both devices using a diffusion process, thus creating two structures which are identical except that the vertical depth of the doping is greater in the novel device.

The attenuation of light passing through the waveguide due to carrier injection was measured in a 2mm long diode structure. Attenuation is directly proportional to the carrier concentration injected into the waveguide region by the forward biased diode. The results of this measurement are shown in figure 7. Line 42 is for the novel structure whereas line 44 is for the comparative structure without recesses. It can be seen that for any given current, the attenuation achieved for the novel diode 42 is approximately 40% greater than for the standard

structure of figure 1. Therefore, it can be inferred that the carrier concentration in the waveguide must also be greater in the novel diode structure as generally predicated by the modeling shown in figures 2-5. Alternatively, to achieve the same level of attenuation a lower injection current is required thereby giving a lower power drain and less local heating. In a further alternative the same attenuation can be achieved for the same current using a physically smaller modulator structure.

The above-described embodiments have all been SOI structures. It is to be expected that application of the invention to non-SOI devices will still give enhanced results although an alternative lower confinement structure will need to be provided.

Further, the above embodiments concentrate on single p and single n junction devices, whereas other diode geometries and other electrical structures such as transistors could also be considered.

It will be appreciated that many variations can be made to the above-described embodiments, without departing from the scope of the present invention.

CLAIMS

1. An electro-optic device including a semiconductor layer in which is formed a waveguide, a modulator formed across the waveguide comprising a doped region on either side, a lower confinement structure for charge carriers beneath the waveguide, lateral confinement structures for charge carriers on either side of the waveguide which extend to the lower confinement structure, at least one of the lateral confinement structures being the doped region to that side of the waveguide, the doped region extending to the lower confinement structure.

2. An electro-optic device according to claim 1 in which both lateral confinement structures are provided by the doped regions on either side of the waveguide.

3. An electro-optic device according to claim 1 in which the semiconducting layer is formed on an insulating layer supported on a substrate.

4. An electro-optic device according to any one of the preceding claims in which the insulating layer is the lower confinement structure.

5. An electro-optic device according to claim 4 in which the lateral confinement structures extend from the base of a recess in the semiconducting layer to the insulating layer.

6. An electro-optic device according to any preceding claim in which one or both doped regions extend from the base of a recess formed in the semiconducting layer.

7. An electro-optic device according to any one of the preceding claims in which the waveguide is covered by an insulating layer.

8. An electro-optic device according to claim 7 as dependent on claim 6 in which the insulating layer extends to at least one side of a recess.

9. An electro-optic device according to any one of claims 5, 6 or 8 in which at least part of the depth of the or each recess has non-vertical sides.

10. An electro-optic device according to any one of the preceding claims in which the doped region to one side of the waveguide is p-type and the doped region to the other side of the waveguide is n-type.

11. An electro-optic device including a semiconducting layer in which is formed a waveguide, a modulator formed across the waveguide comprising a doped region on either side, wherein at least one of the doped regions extends from the base only of a recess formed in the semiconducting layer.

12. An electro-optic device according to claim 11 in which an oxide layer is provided on side walls of the device to inhibit diffusion of dopant therethrough.

13. An electro-optic device according to claim 11 or claim 12 in which the dopant is implanted in the semiconducting layer.

14. An electro-optic device according to any one of the preceding claims in which the waveguide is a rib waveguide.

15. An electro-optic device according to any one of the preceding claims in which a plurality of such lateral modulators are formed along the length of the waveguide, each being a p-i-n modulator, adjacent modulators being mutually reversed in orientation.

16. An electro-optic device according to claim 15 in which there are an even number of modulators.

17. An electro-optic device according to claim 15 in which there are four modulators.

18. An electro-optic device substantially as described herein with reference to and/or as illustrated in the accompanying figures 3 to 7.

Amendments to the claims have been filed as follows

CLAIMS 12

1. An electro-optic device including a semiconductor layer in which is formed a waveguide, a modulator formed across the waveguide comprising a doped region on either side, a lower confinement structure for charge carriers beneath the waveguide, lateral confinement structures for charge carriers on either side of the waveguide which extend to the lower confinement structure, at least one of the lateral confinement structures being the doped region to that side of the waveguide, the doped region extending to the lower confinement structure.

2. An electro-optic device according to claim 1 in which both lateral confinement structures are provided by the doped regions on either side of the waveguide.

3. An electro-optic device according to claim 1 in which the semiconducting layer is formed on an insulating layer supported on a substrate.

4. An electro-optic device according to any one of the preceding claims in which the insulating layer is the lower confinement structure.

5. An electro-optic device according to claim 4 in which the lateral confinement structures extend from the base of a recess in the semiconducting layer to the insulating layer.

6. An electro-optic device according to any preceding claim in which one or both doped regions extend from the base of a recess formed in the semiconducting layer.

7. An electro-optic device according to any one of the preceding claims in which the waveguide is covered by an insulating layer.

which the waveguide is covered by an insulating layer.

8. An electro-optic device according to claim 7 as dependent on claim 6 in which the insulating layer extends to at least one side of a recess.

9. An electro-optic device according to any one of claims 5, 6 or 8 in which at least part of the depth of the or each recess has non-vertical sides.

10. An electro-optic device according to any one of the preceding claims in which the doped region to one side of the waveguide is p-type and the doped region to the other side of the waveguide is n-type.

11. An electro-optic device according to any one of the preceding claims in which the waveguide is a rib waveguide.

12. An electro-optic device according to any one of the preceding claims in which a plurality of such lateral modulators are formed along the length of the waveguide, each being a p-i-n modulator, adjacent modulators being mutually reversed in orientation.

13. An electro-optic device according to claim 12 in which there are an even number of modulators.

14. An electro-optic device according to claim 12 in which there are four modulators.

15. An electro-optic device substantially as described herein with reference to and/or as illustrated in the accompanying figures 3 to 7.

16. An electro-optic device according to claim 15 in which there are an even number of modulators.

17. An electro-optic device according to claim 15 in which there are four modulators.

18. An electro-optic device substantially as described herein with reference to and/or as illustrated in the accompanying figures 3 to 7.

INVESTOR IN PEOPLE

Application No: GB 0104384.3 **Examiner:** Helen Edwards
Claims searched: 1-10 14-18 15 **Date of search:** 24 October 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): G2F: FCW

Int Cl (Ed.7): G02F: 1/025

Other: Online database: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	GB 2340616 A (BOOKHAM TECHNOLOGY LIMITED) See figure 2	1, 2, 3, 4, 7, 10, 14
A	GB 2265252 A (BOOKHAM TECHNOLOGY LIMITED)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

INVESTOR IN PEOPLE

Application No: GB 0104384.3 16 **Examiner:** Helen Edwards
Claims searched: 11 to 13 **Date of search:** 30 January 2002

Patents Act 1977
Further Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): G2F: FCW

Int Cl (Ed.7): G02F: 1/025

Other: Online database: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	NONE	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.